What is claimed is:

1. A multi-chip package, comprising:

a plurality of pins; and

first through Nth semiconductor chips, each of which includes,

an input/output pad,

an input/output driver coupled to the input/output pad,

an internal circuit, and

an internal pad for coupling the input/output driver and the internal circuit,

wherein the internal pads of the first through Nth semiconductor chips are coupled to each other,

wherein the input/output pad of the first semiconductor chip directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package, and

wherein the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, which are coupled to each other.

2. The multi-chip package as claimed in claim 1, wherein the internal pads are coupled to each other via a common pad installed at a substrate.

3. The multi-chip package as claimed in claim 1, wherein the input/output pad of the first semiconductor chip is bonded to one of the pins of the multi-chip package.

4. The multi-chip package as claimed in claim 1, wherein each of the first through (N-1)th semiconductor chips includes a delay circuit for receiving the input/output signal simultaneously with the internal circuit of the Nth semiconductor chip.

5. A multi-chip package, comprising:

a plurality of pins; and

first through Nth semiconductor chips, each of which includes,

an input/output pad,

an input/output driver coupled to the input/output pad,

an internal circuit, and

an internal pad for coupling the input/output driver and the internal circuit,

wherein the internal pads of the first through Nth semiconductor chips are coupled to each other,

wherein the input/output pad of the first semiconductor chip directly receives an input/output signal transmitted via a corresponding one of the pins of the multi-chip package,

wherein the second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads, which are coupled to each other, and

wherein the first through Nth semiconductor chips include direct input/output pads which directly receive external signals input via corresponding pins of the multi-chip package.

6. The multi-chip package as claimed in claim 5, wherein the internal pads are coupled to each other via a common pad installed at a substrate.

7. The multi-chip package as claimed in claim 5, wherein the input/output pad of the first semiconductor chip is bonded to one of the pins of the multi-chip package.

8. The multi-chip package as claimed in claim 5, wherein each of the first through (N-1)th semiconductor chips includes a delay circuit for receiving the input/output signal simultaneously with the internal circuit of the Nth semiconductor chip.

9. The multi-chip package as claimed in claim 5, wherein the external signals are transmitted at a lower speed than the input/output signal.

10. A multi-chip package, comprising:

a plurality of pins; and

first through Nth semiconductor chips, each of which includes,

first through Nth (N is a natural number) input/output pads,

first through Nth input/output drivers coupled to the input/output pads,

an internal circuit, and

first through Nth internal pads for coupling the input/output drivers with the internal circuit,

wherein the first through Nth internal pads of the first semiconductor chip are coupled to the first through Nth internal pads corresponding thereto of the second through Nth semiconductor chips,

wherein first through Nth input/output signals are received via corresponding ones of the pins of the multi-chip package, and one input/output signal for each semiconductor chip is received by the corresponding input/output pad, and

wherein the first through Nth semiconductor chips indirectly receive the other input/output signal via the corresponding internal pads, coupled to each other.

11. The multi-chip package as claimed in claim 10, wherein the first through Nth internal pads are coupled to each other via first through Nth common pads installed at a substrate.

12. The multi-chip package as claimed in claim 10, wherein the first through Nth semiconductor chips include delay circuits for controlling delay times of the input/output signals, such that the input/output signals received by the first through Nth semiconductor chips are simultaneously input to the respective internal circuits.

13. The multi-chip package as claimed in claim 10, wherein the first through Nth semiconductor chips further include direct input/output pads which directly receive external signals input via corresponding pins of the multi-chip package.

14. The multi-chip package as claimed in claim 13, wherein the external signals are transmitted at a lower speed than the input/output signal.

15. A multi-chip package, comprising:

a plurality of pins; and

first through Nth semiconductor chips, each of which includes,

a plurality of input/output pads,

a plurality of input/output drivers coupled to the input/output pads,

an internal circuit, and

internal pads for coupling the input/output drivers with the internal circuit,

wherein a total number of internal pads equals that of the input/output drivers,

wherein the plurality of internal pads of the first semiconductor chip are coupled to the plurality of internal pads corresponding thereto of the second through Nth semiconductor chips,

wherein among first through Mth (M>N, M is a natural number) input/output signals received via corresponding pins of the multi-chip package, a certain number of the input/output signals are transmitted directly to the input/output pads of the first through Nth semiconductor chips, and

wherein the first through Nth semiconductor chips indirectly receive the other input/output signals via the corresponding internal pads of the first through Nth semiconductor chips.

16. The multi-chip package as claimed in claim 15, wherein the plurality of internal pads are coupled to each other via a plurality of corresponding common pads installed at a substrate.

17. The multi-chip package as claimed in claim 15, wherein the first through Nth semiconductor chips include delay circuits for controlling delay times of the input/output signals, such that the input/output signals received by the first through Nth semiconductor chips are simultaneously input to the respective internal circuits.

18. The multi-chip package as claimed in claim 15, wherein the first through Nth semiconductor chips further include direct input/output pads which directly receive external signals input via corresponding pins of the multi-chip package.

19. The multi-chip package as claimed in claim 15, wherein the external signals are transmitted at a lower speed than the input/output signal.